



DX-LR03-900T30D

Module technical manual

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1. Module Introduction

1.1. Overview

The DX-LR03-900T30D is a low-power, ultra-long-range LoRa module. It is developed by SHEN ZHEN DX-SMART TECHNOLOGY CO.,LTD., for intelligent wireless data transmission. It adopts the domestic ASR6601 SoC chip. Inside the chip, there is an integrated Sub 1GHz radio frequency transceiver, an Arm China STAR-MC1 microprocessor, built-in Flash memory, and SRAM. With an external high-power PA, it has an ultra-large output power of up to 28dbm. This module supports interfaces such as UART, I2C, and I2S, as well as IO port control and ADC acquisition. It features low power consumption, high performance, and long-range capabilities. It is suitable for a variety of application scenarios in the IoT field, such as smart meters, intelligent logistics, smart buildings, smart cities, smart agriculture, and many other application scenarios.

1.2. Features

Core and Memory:

- Arm China STAR-MC1 architecture
- 32-bit ARM STAR core with a maximum frequency of 48MHz
- High power PA, super output power: +28dBm
- Receiver sensitivity: -125dBm (125K, SF7)

A peripheral interface:

- Support UART, I2C, I2S, LPUART, SSP, QSPI and other interfaces

Module parameters:

- Operating voltage: 4V-5.5V (typical value: 5V)
- Support working frequency range: 850-931MHz
- Support for sleep mode
- External antenna
- The open visible distance can reach 10km (for reference only, the actual distance is subject to the actual measurement)
- Working temperature: -40~+85 °C

Note: the antenna needs to be connected before the module is powered on to avoid no-load

1.3. Applications

- Smart meter meter
- Smart logistics
- Smart buildings
- Smart cities

1.4. Functional block diagram

Below for DX - LR03-900 t30d module of function block diagram, expounds the main functions as follows:

- Power supply part
- Baseband part
- Memory
- Rf part
- Peripheral interface

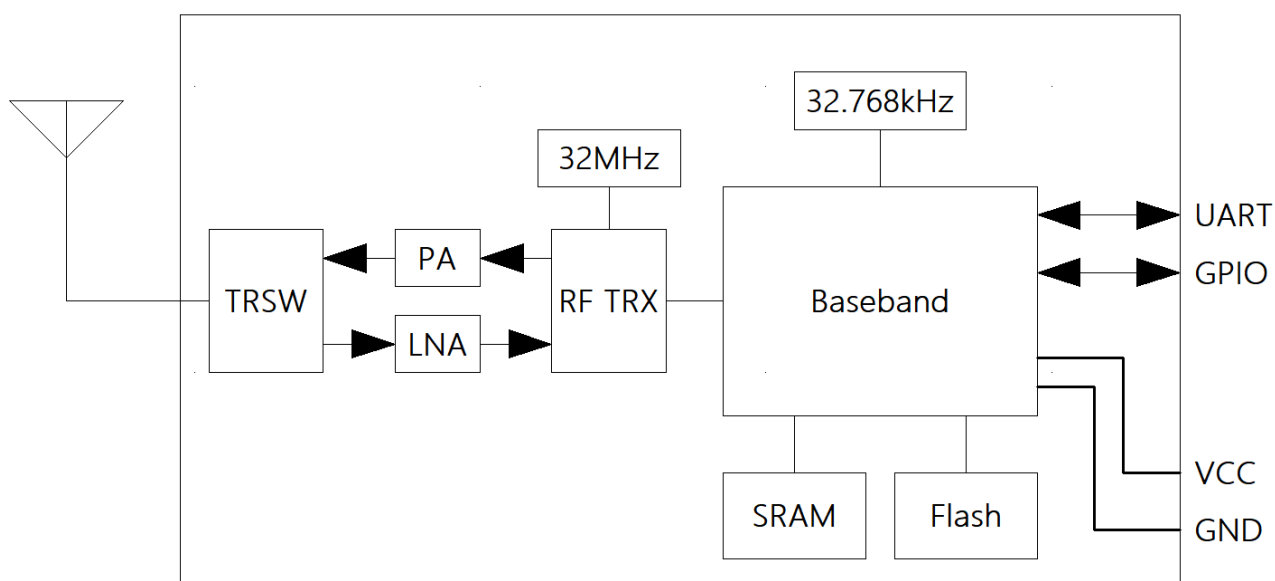




Figure 1: Functional block diagram 1



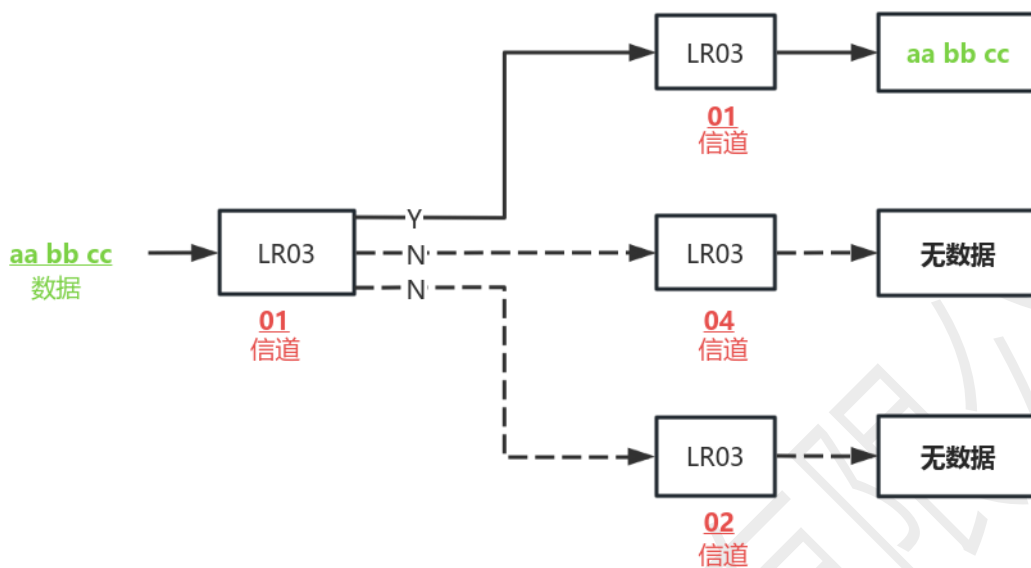
1.5. Basic parameters

Table 1: Table of basic parameters1

The parameter name	Details	Parameter names	Details
Chip model	ASR6601	Module model	DX-LR03-900T30D
Modulation	Spread spectrum modulation	Module size	43.0(L) x 28.0 (W) x3.2(H) mm
Operating voltage	4-5.5V (Typical value: 5V)	Frequency band	850-931MHz
Sensitivity	-125dBm (125k, SF7)	Transmit power	0~+28dBm
Rf input impedance	50 Ω	Hardware interface	LPUART
Antenna port	External antenna		

1.6. Transmission method

- Transparent transmission: the sender and the receiver can transmit data with the same channel



信道 channel

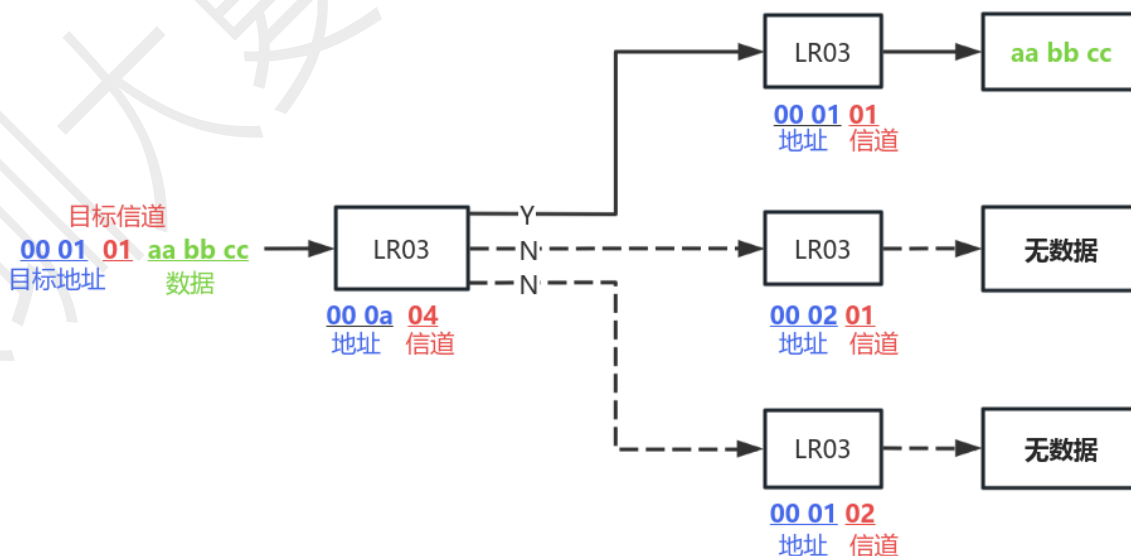
数据 data

无数据 no data

Figure 2: Transparent transmission2

- Fixed-point transmission: When the sender sends data, the target address and target channel contained in the data should be the same as the address and channel of the receiver.

Data format, such as: the target address (hexadecimal, two bytes) + target channel (hexadecimal, one byte) + data (hexadecimal)





目标信道 Target channel

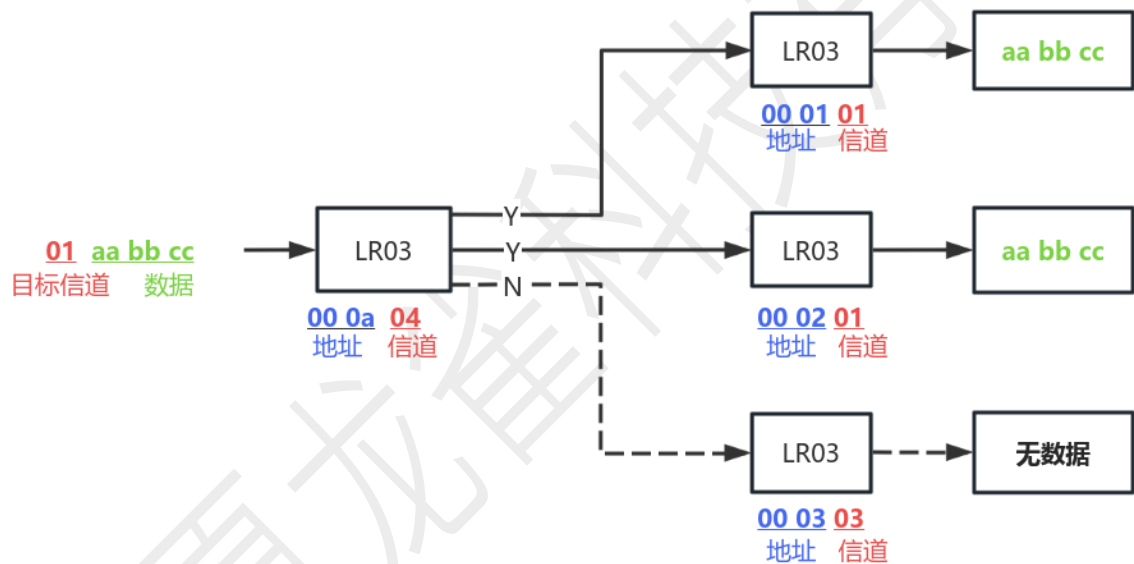
地址 address

数据 date

无数据 no date

Figure 3: Fixed-point transmission3

- Broadcast transmission: When the sender sends data, the target channel in the data should be the same as the channel at the receiver.
Data format such as: target channel (one byte, hexadecimal) + data (hexadecimal)



目标信道 Target channel

地址 address

数据 date

无数据 no date

Figure 4: Broadcast transmission4



2. Application interface

2.1. Module pin definition

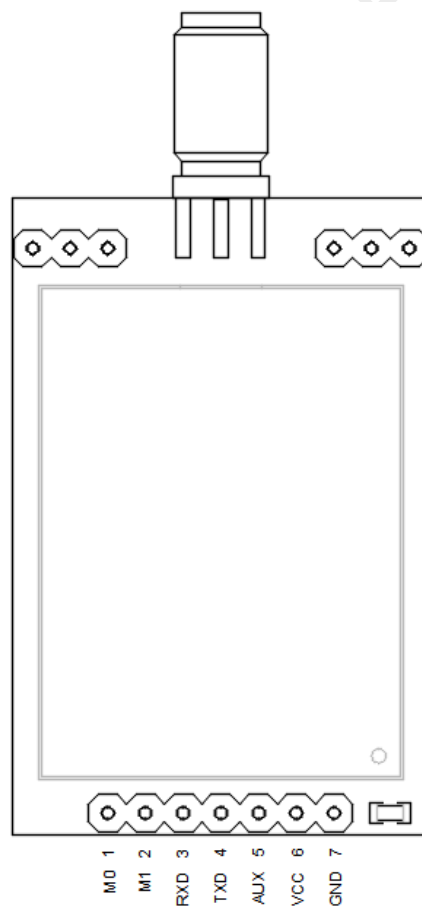


Figure 5: Module pin definition5

2.2. Illustration of the pin definition

Table 2: Pin Definition Instructions Table 2

Pin serial number	Pin name	Pin function	Instructions
1	M0	Set aside	Customizable IO ports
2	M1	Sleep mode controls the foot	Low: Enter sleep mode High: Wake up sleep mode
3	RXD	Serial port data input	-
4	TXD	Serial port data output	-
5	AUX	Module RF status indicator foot	Refer to 2.3.3 for details
6	VCC	Power input pin	5V(typical value)
7	GND	Power ground	-

2.3. Power supply design

2.3.1. Power port

Table 3: Power interface pin definition Table3

Pin names	Pin number	Description	Minimum value	Typical value	Maximum value	Units
VCC	6	Module power supply	4	5	5.5	V
GND	7	to	-	0	-	V

2.3.2. Power supply stability Requirements

DX - LR03-900 t30d power supply in the range of 4 ~ 5.5 V, need to ensure that not less than 4 V input voltage. Below is the VCC voltage dips in radio frequency burst transmission.

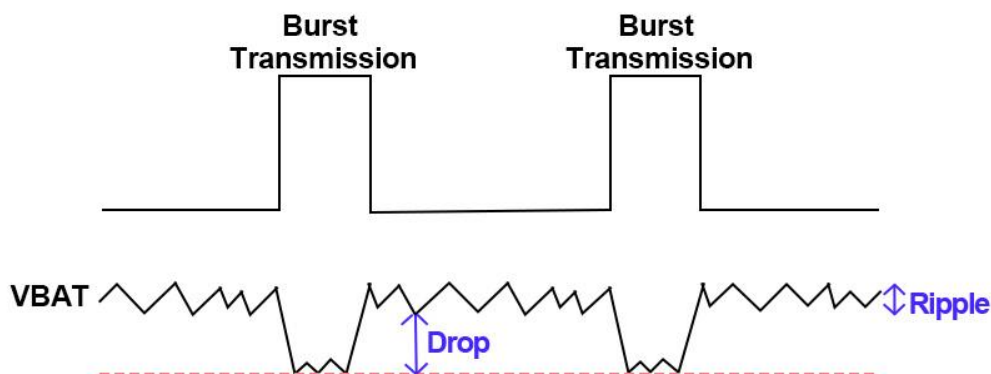


Figure 6: Burst transmission power requirements⁶

In order to reduce the voltage drop, it is recommended that the reserved for VCC 2 (22 uF, 0.1 uF) which has the best ESR performance of chip multilayer ceramic capacitors (MLCC), and capacitance placed close to the VCC pin.

2.3.3. AUX module rf status indicates the feet

- Low: The module is currently in the receiving idle or data transmitting idle state, can transmit data, or is waiting for pairs
The end module sends the data.
- High level: the module's current in the data to receive or send data accumulation state, please wait for the feet into a low level.

2.4. Power consumption

- Sleep mode: In this mode, both MCU and RF go to sleep. Use foot wake and sleep, M1 foot pull up to wake up, M1 foot pull down to sleep.
- Air wake mode: the mode, the module for four seconds a cycle test CAD (overall sleep time is: 4 s minus CAD test time), such as module detected data, will enter the receive mode, after receiving the data, automatically entered into dormancy. Don't sleep during the dormancy, rf dormancy, MCU. The model can be written to save.
- High aging mode: In this mode, the module is always in the receiving state and can receive data from other devices at any time. When the serial port of the module receives

the data from the master control, it switches to the transmitting state, and transmits the data out. After the transmission is completed, it switches back to the receiving state.

Table 4: Power consumption table4

Operating status	Status	Current	Unit
Sleep mode	Standby	2.61	mA
Air wake-up mode	Standby	6.75	mA
	Receive	48.71	mA
High time mode	standby	22.28	mA
	Receive	26.42	mA
	Transmission	179	mA

Notes

The data in the table are measured when the module is at LEVEL=0 and the frequency band is 868Mhz.

2.5. Hardware physical interface

2.5.1. General purpose digital IO port

There are 47 universal digital IO ports defined in the module. All these IO ports can be configured by software to implement various functions, such as button control, LED drive or interrupt signal of the main controller. Keep hung up when not in use.

2.5.2. I2C interface

ASR6601 including a I2C host mode, support model of standard rate (100 KBPS) and fast (400 KBPS), and support multiple hosts and bus arbitration function. The SDA for data transmission, SCL clock line for reference.

When the software starts to perform read or write operations, I2C switches from the default slave receive mode to the host send mode. The Start condition is followed by a 7-bit slave address and a 1-bit R/nW. Upon receiving the ACK, the I2C enters one of the following two modes: host send mode -write data, and host receive mode -read data.

Write I2Cx_CR CPU registers to start a host affairs. FIFO mode is used only in host mode. FIFO mode can be used to send and receive, to help reduce I2Cx_DBR register air is broken and full of interruption, FIFO allowed to read and write more bytes without interruption after each byte operation CPU.

The following figure shows the I2C timing diagram, which is the same as the I2C slave timing diagram.

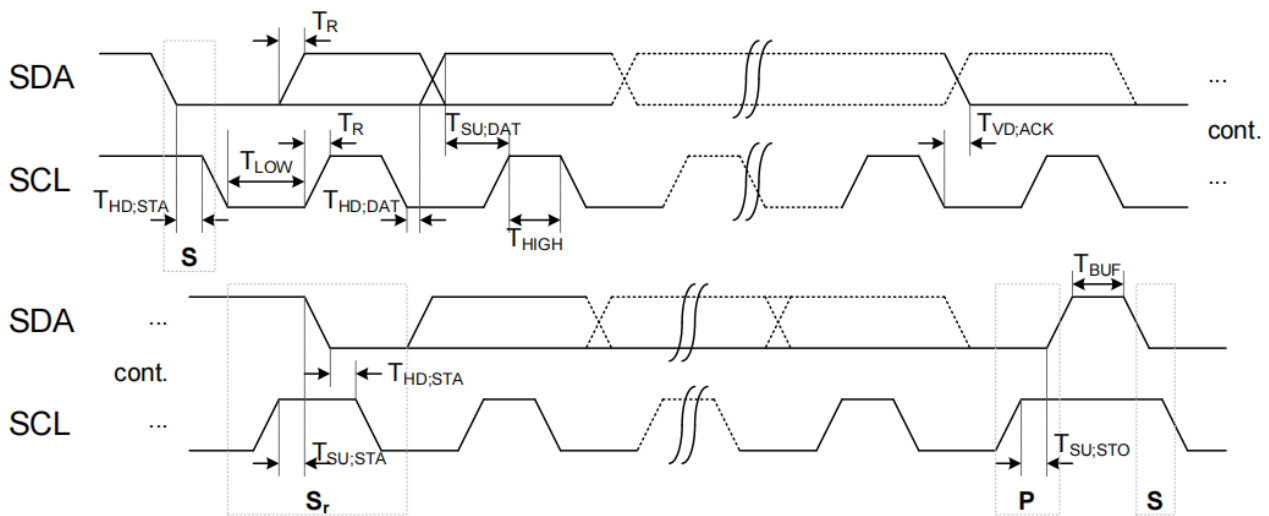


Figure 7: IIC communication timing diagram7

ASR6601 also includes an I2C slave mode, support model of standard rate (100 KBPS) and fast (400 KBPS).

In which slave receive is the default mode, I2Cx_CR{UE} must be set to 1, and I2C monitors the Start condition on the bus. If the Start condition is detected, the interface reads the first 8 bits of data and compares the first 7 bits with its slave address. If the first 8 bits (R/nW) of the first byte is low, then the I2C stays in slave receive mode and the I2Cx_SR{SAD} is clear 0. If R/nW is high, I2C switches to the slave transmit mode and sets I2Cx_SR{SAD} to 1.

As the receiving slave, I2C pulls the SDA line low to generate ACK when SCL is high and sends it to the host.

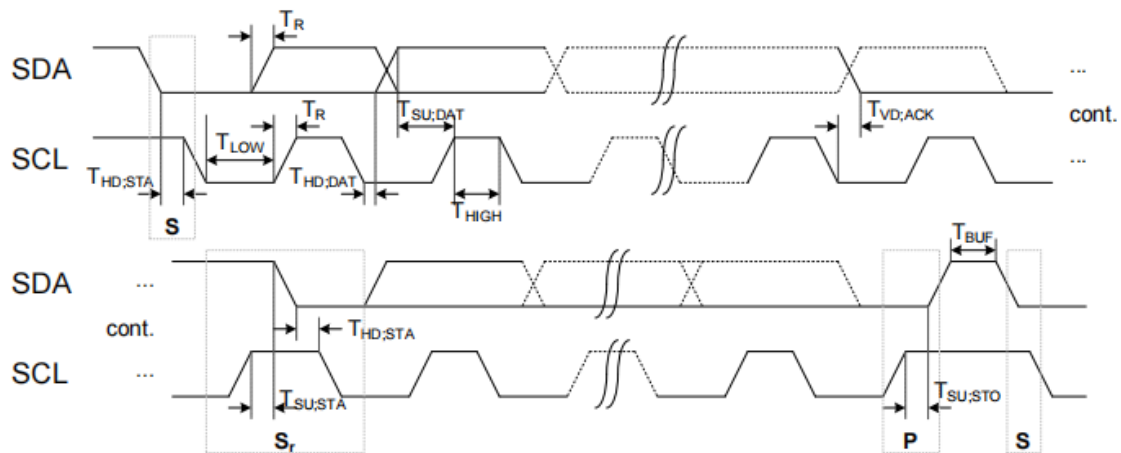


Figure 8: I2C from machine sequence diagrams8

2.5.3. UART interface

The ASR6601 supports UART and IrDA modes. Transmit and receive FIFO independent, 16 bit baud rate divisors integer part and 6 bit baud rate divisors decimal part. Standard asynchronous communication bit, support 5, 6, 7 and 8 bits of data, support parity check, support 1 or 2 stop bits. Support DMA, support false start bit detection, support Line Break generation and detection, support hardware flow control. Can register by ID uniquely identify each UART port.

The frequency of UARTCLK must meet the requirements of baud rate produced: $F_{UARTCLK}(\text{min}) \geq 16 \times \text{baudrate}(\text{Max})$, $F_{UARTCLK}(\text{Max}) \leq 16 \times 65535 \times \text{baudrate}(\text{min})$.

For example, to generate between 110 to 460800 baud rate, the frequency of UARTCLK must be between 7.3728 MHz and 115.34 MHz.

At the same time, UARTCLK must not be greater than 5/3 times PCLK: $F_{UARTCLK} \leq \frac{5}{3} * F_{PCLK}$.

The sending and receiving Fifos are independent, which can be switched on or off through the wired register `UARTx_LCR_H{FEN}`. Send 16 x 8, receive 16 x 12, receive FIFO has a status code of 4 bits per character, FIFO water level can be configured to 1/8, 1/4, 1/2, 3/4 and 7/8 through FIFO interrupt water level selection register `UARTx_IFLS`, when FIFO disabled is equivalent to depth 1. The FIFO status is obtained by querying the flag register `UARTx_FR`.

IrDA SIR ENDEC provides the function of converting between UART data stream and half-duplex serial SIR Interface, data from UART encoded output and decoded input to UART, there are two modes: ·

In IrDA mode, the logic 0 level is converted to a high level pulse of width 3/16 of the nSIROUT baud rate bit period, and the logic 1 level is converted to a low level. ·

Low-Power IrDA mode, the transmitted high level pulse width is 3 times the internal IrLPBaud16 cycle (1.63us, assuming a nominal frequency of 1.842MHz). The physical layer of IrDA SIR Is a half-duplex communication link, and the delay between transmission and reception should be maintained at least 10ms. This delay must be done by software because UART does not support automatic delay.

The following image shows the effect of IrDA 3/16 data modulation:

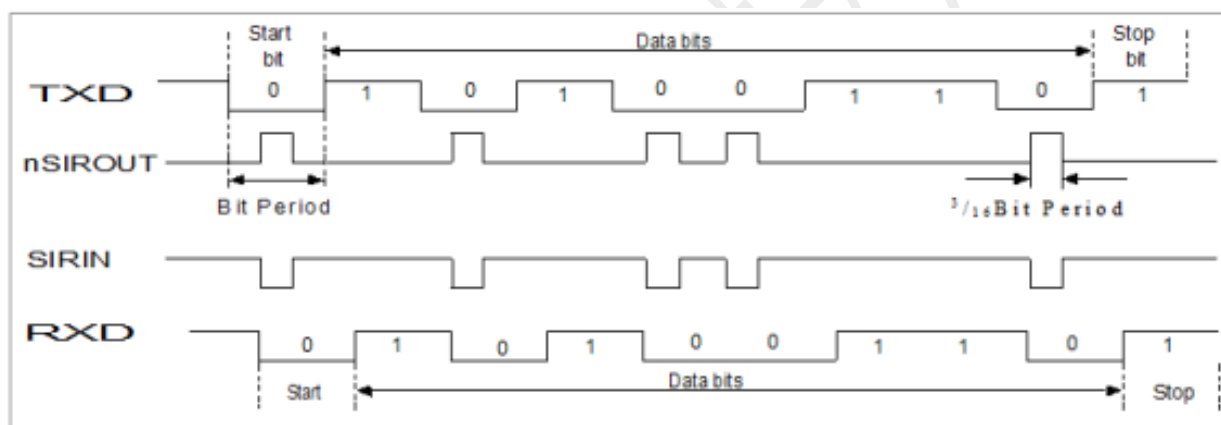


Figure 9: IrDA data modulation

The UART is enabled through the UARTx_CR{UARTEN}, through the configuration data bit, stop bit, parity and other parameters of the wired register UARTx_LCR_H.

When the receive is idle, the UARTRXD pulls low, Baud16 enables the receive counter to start counting, and the UART mode starts sampling in the 8th counting cycle. IrDA mode starts sampling in the fourth count cycle to allow for shorter logic 0 pulses.

If UARTRXD remains low at the eighth counting cycle, then a valid start bit is detected; otherwise, it is judged false and is ignored.

If the start bit is valid, the data is sampled every 16 Baud16 cycles, and the length is determined by UARTx_LCR_H{WLEN}. If parity is enabled, a parity bit comparison is performed.

Finally, when the UARTRXD becomes high, the valid stop bit is acknowledged, otherwise a frame error occurs. The fully received character is deposited into the receive FIFO along with the error bit.

2.5.4. SSP Interface

The ASR6601 supports the SSP interface, which is a synchronous serial interface that supports both MASTER and SLAVE modes. Multiple frame formats are supported, and the data width and output rate can be configured as needed. The maximum output is 16MHz, and TX/RX FIFO with 16-bit width and depth of 8 is supported.

The SSP has 4 main pins: SSP_NSS, SSP_CLK, SSP_TX, and SSP_RX.

- SSP_NSS: SSP slice selection signal, low effective.
- SSP_CLK: SSP clock signal, clock output for MASTER mode and clock input for SLAVE mode.
- SSP_TX: The SSP sends the signal, whether in MASTER mode or SLAVE mode, it sends the pin.
- SSP_RX: The SSP receives the signal, whether in MASTER mode or SLAVE mode, it is the receiving pin.

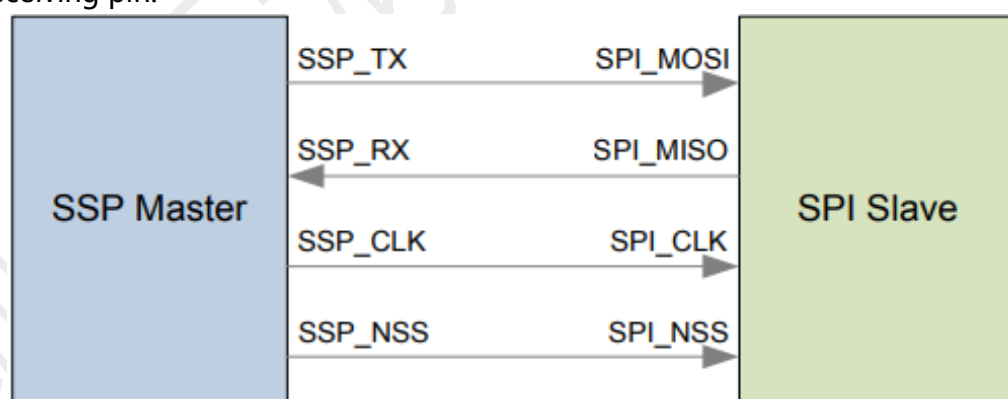


Figure 10: Connection between SSP master and SPI slave10

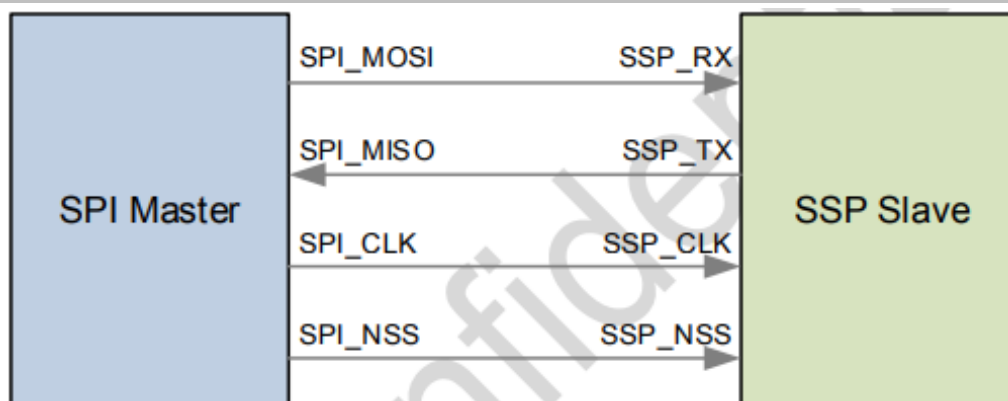


Figure 11: Connection between SPI slave and SSP master11

SSP Clock Constraints:

- The maximum supported output clock is 16MHz
- The maximum clock in MASTER mode is 1/2 of PCLK
- The maximum clock in SLAVE mode is 1/12 of PCLK

SSPCLK is the interface clock of the SSP, SSPCLKOUT is the output clock of the SSP. Take the default 24MHz as an example, if you want to output a 1MHz clock, set CPDVR to 2 and SCR to 11.

2.5.5. LPUART

The ASR6601 includes the LPUART interface, which is a low-power serial port peripheral that supports baud rates up to 9600 at 32K clocks. In the very low power mode, the LPUART can also be woken up by the received data. LPUART supports CTS/RTS flow control and DMA requests.

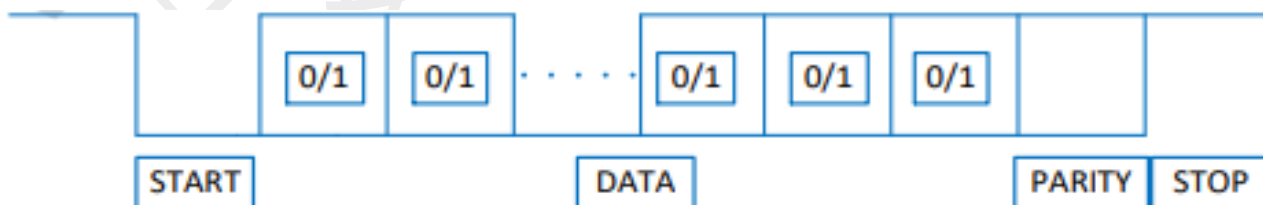


Figure 12: Data transfer format of LPUART12

When idle, LPUART's data lines should be kept high. During DATA transmission, the START bit (START), data bit (DATA), PARITY bit (PARITY) and STOP bit (STOP) are transmitted in sequence.

The meaning of each bit is as follows:

- Start bit: A 0 signal is first sent to indicate the beginning of data transmission.
- Data bits: 5-8 bits are transmitted in sequence, depending on the configuration.
- Parity bits: After the data bits, transmit a parity bit of one bit, which can also be configured to have no parity bits.
- Stop bit: A sign that the data transmission is over. It can be 1 or 2 bits.

The configuration of LPUART baud rate supports fractional frequency division, which is mainly configured by LPUART_BAUD_RATE_INT and LPUART_BAUD_RATE_FRA two registers. Taking the clock frequency of the LPUART interface as 32.768KHz, the baud rate as 9600 as an example, and the frequency division factor as $32768/9600=3.413$, the register LPUART_BAUD_RATE_INT is configured as 3, and the register LPUART_BAUD_RATE_FRA is configured as 7 ($0.413 \times 16 = 6.608$, rounded to 7).

The connection between the two LPUARTs is as follows:

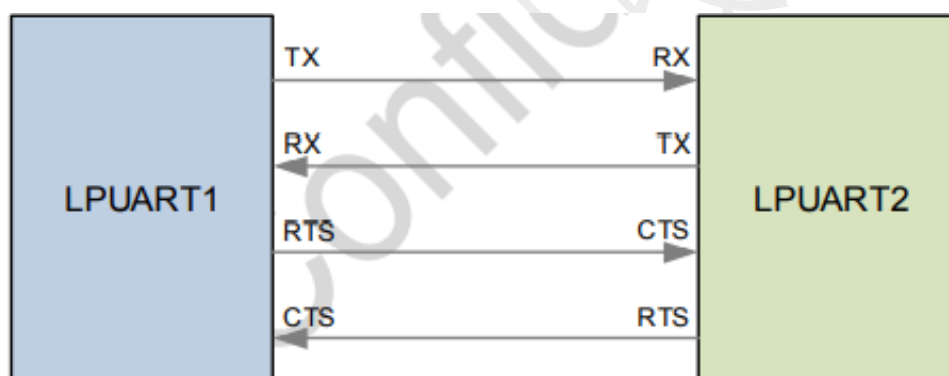


Figure 13: Connection between two LPUART devices

Where RTS is the output signal, which is used to indicate that this device is ready to receive data, the low level is valid, and the low level indicates that this device can receive data. CTS is the input signal, which is used to determine whether it can send data to the other party. The low level is valid, and the low level indicates that the device can send data to the other party.

LPUART low power wake-up includes RX low level wake-up, effective START wake-up, RX_DONE wake-up. The wakeup mode is enabled by configuring the LPUART_WAKEUP_EN bit of the LPUART_CR0 register.

2.5.6. Analog-to-digital Converter (ADC)

The ADC is a 12-bit analog to digital converter, which supports 8 external channels and 7 internal channels. The internal channel can collect VBAT/3 and support up to 1M sampling rate. Both single-ended and differential modes are supported. The single-ended range is 0.1V~1.1V, and the differential range is -1.0~1.0V. 16 sampling sequences can be configured to support continuous, single and non-continuous sampling modes. Support software trigger and hardware trigger, trigger source can be configured. Support DMA request and interrupt request.

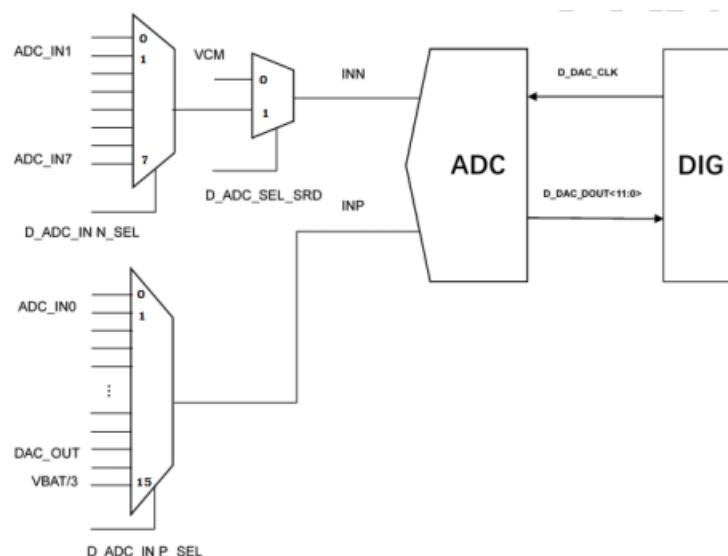


Figure 14: Block diagram of ADC14

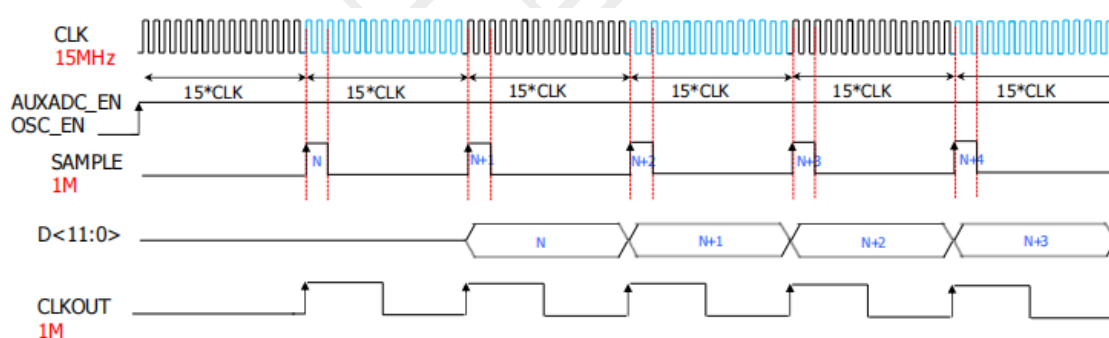


Figure 15: Timing diagram of a 12-bit ADC15

Support configuration for single-ended and differential mode. External channel supports single end and differential mode, internal channel only supports single end mode. Differential is a fixed combination, does not support random pairing, where 0/1 channel for a group, 2/3 channel for a group, 4/5 channel for a group, 6/7 channel for a group. Single-ended and differential control is different only in the sampling phase, and there is no difference in the maintenance phase. In the final data, the most significant bit of differential input is the sign bit (11bit data bit, 1

sign bit), and the single-ended input is 12bit data bit, no sign bit. The input mode is configured through the sampling channel differential/single-ended select register ADC_DIFFSEL.

Configure the sampling mode via ADC_CFGR{CONV_MODE} : The sampling sequence configuration is supported, the sampling sequence is up to 16 channels, both single-ended and differential channels can be configured. Differential mode, the sampling sequence can be configured only with P terminal. The sampling channel can configure the same channel repeatedly to decide to sample the channel multiple times per sequence. The sampling sequence is configured through the channel sampling sequence control registers ADC_SEQR0 and ADC_SEQR1, and one sampling channel is configured every 4 bits. The two 32-bit registers have a total of 64 bits, and a maximum of 16 sampling channels can be configured. •

- Continuous sampling: Once the trigger is effective, it starts to continuously transform the selected input sequence, and automatically starts a new cycle after the completion of each round, until the software configuration stops. •
- Single sampling: Each trigger executes a sampling sequence cycle, and the sampling completes automatically. •
- Non-continuous sampling: each ADC conversion in the sequence needs to be triggered by hardware or software. If a sequence is finished, the trigger again starts from the beginning of the sequence; In the continuous and single mode, each trigger will complete a complete sequence.

2.6. Reference Connected circuit

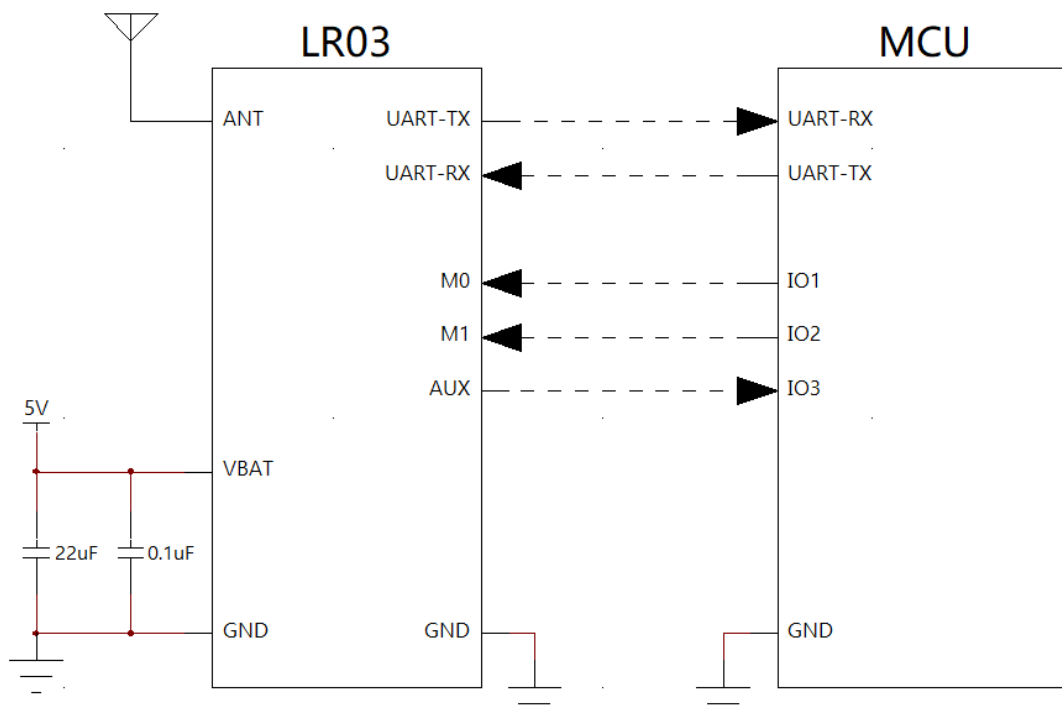


Figure 16: Typical application circuit16

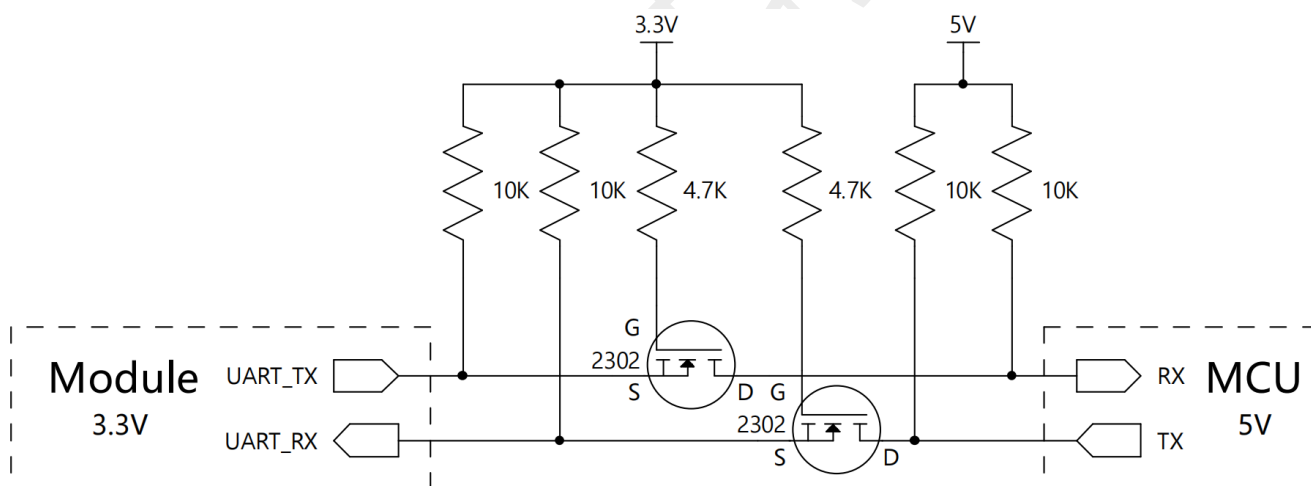


Figure 17: Serial port level conversion reference circuit17

3. Electrical characteristics, RF characteristics and reliability

3.1. Maximum rating

Pressure in excess of the absolute maximum rating may cause permanent damage to the equipment. These are stress ratings only and therefore do not imply functional operation of the equipment under these or any other conditions beyond those indicated in the operating section of the instruction manual. Prolonged exposure to absolute maximum rating conditions may affect the reliability of the equipment.

Table 5: Absolute Maximum Rating Table5

Parameters	Minimum	Maximum	Units
VBAT	-0.2	5.5	V
I/O supply voltage (VDDIO)	-0.2	3.7	V
Storage temperature range	-40	+125	°C

Table 6: Recommended conditions of use6

Parameters	Minimum value	Typical value	Maximum value	Units
VBAT	4	5	5.5	V
I/O supply voltage (VDDIO)	3	3.3	3.7	V
Operating temperature range (TA)	-40	+25	+85	°C

3.2. Static protection

In the application of modules, due to the static electricity generated by human body static electricity and charged friction between microelectronics, it may cause some damage to the module through various ways, so ESD protection should be paid attention to. ESD protection measures should be taken in the process of research and development, production, assembly and

testing, especially in product design. For example, at the interface of the circuit design and the point susceptible to electrostatic discharge damage or influence, anti-static protection should be increased, and anti-static gloves should be worn in production.

Table 7: Table of ESD tolerant voltage of module pins7

Test interface	Contact discharge	Air discharge	Units
VBAT and GND	+4	+8	kV
Main antenna interface	+2.5	+4	kV

4. Mechanical dimensions and layout suggestions

This section describes the mechanical dimensions of the module, all dimensions are in millimeters; All dimensions not marked with tolerances with tolerances of ± 0.3 mm.

4.1. Modular mechanical ruler

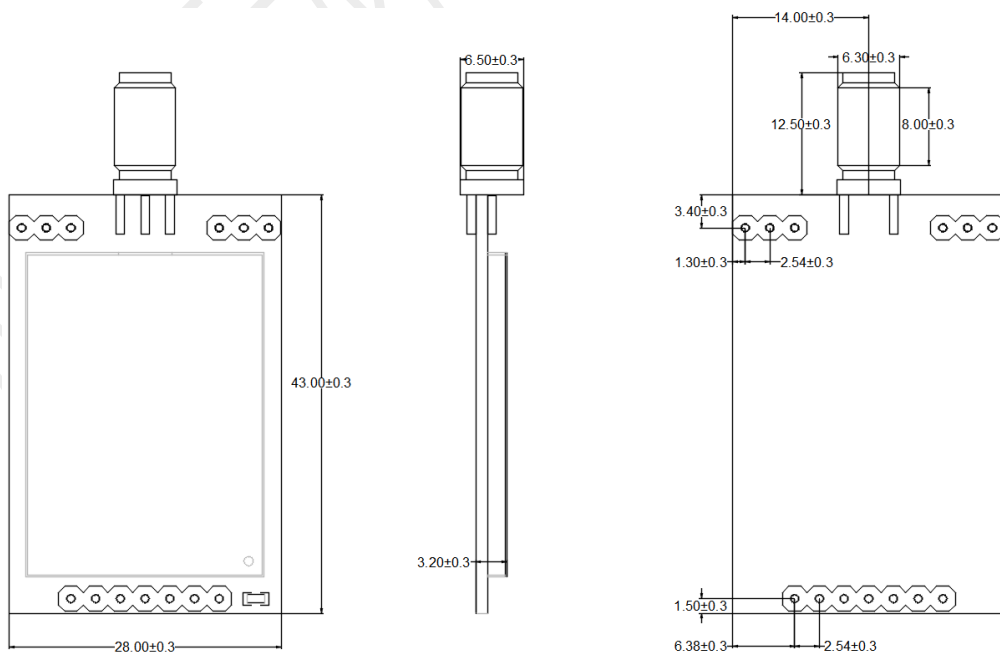




Figure 18: Top view, side view and bottom view dimensions of the module18

4.2. Recommended packaging

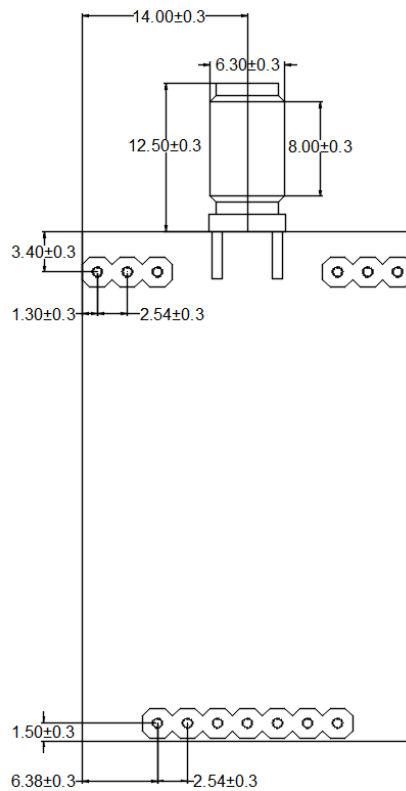


Figure 19: Bottom view of proposed package size19

4.3. Module top view/bottom view

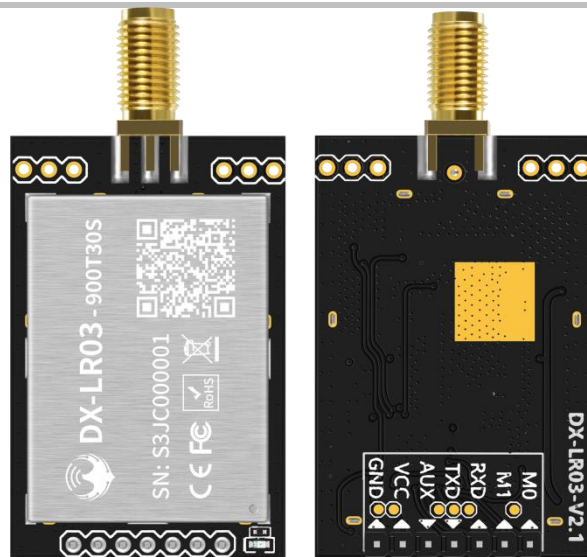


Figure 20: Module top view and bottom view20

Notes

The above picture is for reference only, please refer to the actual product appearance and label information of the module.

4.4. Hardware design layout suggestions

The DX-LR03-900T30D module works at 850-931MHz and uses an external antenna. The standing Wave ratio (VSWR) and efficiency of the antenna depend on the position of the patch. The influence of various factors on the wireless transceiver signal should be avoided as much as possible.

1. Avoid using metal to enclose the product shell of DX-LR03-900T30D. When using part of the metal shell, try to keep the module antenna part away from the metal part. Product internal metal connection wire or metal screws, should be as far away from the module antenna part.
2. The module antenna part should be placed on the edge of the carrier board PCB or directly exposed to the carrier board, try not to be placed in the middle of the board.
3. It is recommended to use insulating materials to isolate the module mounting position on the substrate, such as putting a whole screen print (TopOverLay) at the position.

5. Storage and packaging

5.1. Storage conditions

Modules are shipped in vacuum-sealed bags. The module has a humidity sensitivity class of 3 (MSL 3), and its storage is subject to the following conditions:

1. Recommended storage conditions: temperature $23\pm 5^{\circ}\text{C}$ and relative humidity of 35~60%.
2. Under the recommended storage conditions, the module can be stored in a vacuum sealed bag for 12 months.
3. The unsealed workshop life of the module is 168 hours under workshop conditions of $23\pm 5^{\circ}\text{C}$ and relative humidity below 60%. Under these conditions, the module can be directly used for reflux production or other high temperature operation. Otherwise, it is necessary to store the module in an environment with relative humidity less than 10% (for example, a moistureproof cabinet) to keep the module dry.
4. If the module is under the following conditions, it is necessary to pre-bake the module to prevent the PCB blistering, cracking and delamination after the module is hygro-absorbed and then welded at high temperature:
 - Storage temperature and humidity do not meet the recommended storage conditions
 - The module fails to complete production or storage according to Clause 3 above after unpacking
 - Vacuum packaging leakage, materials in bulk
 - Before module repair

5.2. Packing Specifications

The DX-LR03-900T30D module is packaged in a pallet and enclosed in a vacuum sealed bag with desiccants and humidity cards. Each tray is 270*200*22.5mm in size and contains 20 modules. The specifications are as follows:

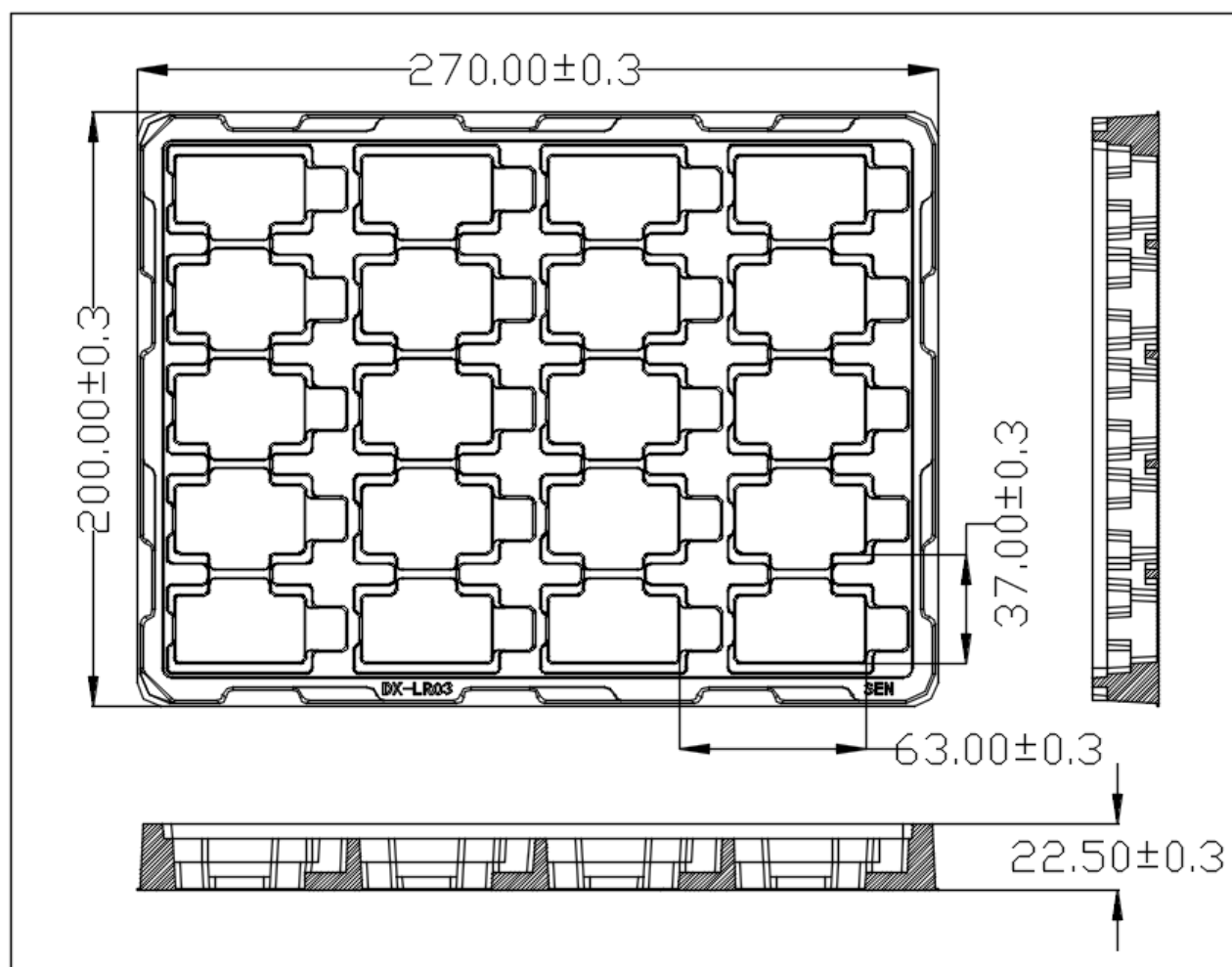


Figure 21: Pallet dimensions (in millimeters)